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(54) **SEMICONDUCTOR PACKAGE COMPRISING TWO SEMICONDUCTOR MODULES AND LATERALLY EXTENDING CONNECTORS**

(71) Applicant: **Infineon Technologies AG**, Neubiberg (DE)

(72) Inventors: **Olaf Hohlfeld**, Warstein (DE); **Juergen Hoegerl**, Regensburg (DE); **Gottfried Beer**, Nittendorf (DE); **Magdalena Hoier**, Seubersdorf (DE)

(73) Assignee: **Infineon Technologies AG**, Neubiberg (DE)

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H01L 25/065	(2006.01)
H01L 23/00	(2006.01)
H01L 23/31	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/563*** (2013.01); ***H01L 23/3135*** (2013.01); ***H01L 24/24*** (2013.01); ***H01L 24/82*** (2013.01); *H01L 23/3107* (2013.01); *H01L 2224/04105* (2013.01); *H01L 2224/24137* (2013.01); *H01L 2224/73267* (2013.01); *H01L 2924/1033* (2013.01); *H01L 2924/10253* (2013.01); *H01L 2924/10272* (2013.01); *H01L 2924/1203* (2013.01); *H01L 2924/13055* (2013.01); *H01L 2924/13091* (2013.01)

(58) **Field of Classification Search**

USPC 257/678–740, 787–796, 257/E23.001–E23.194

See application file for complete search history.

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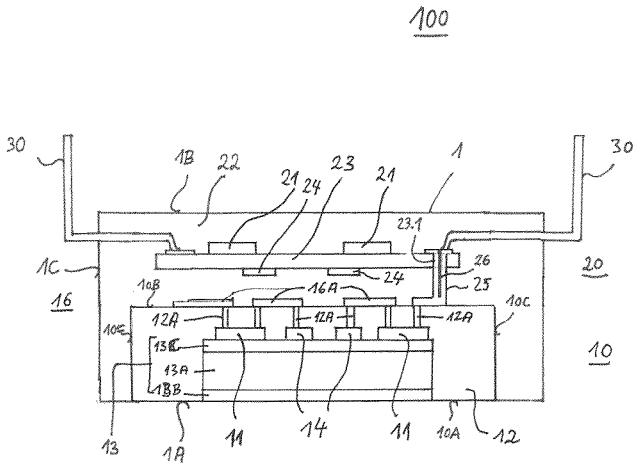
Primary Examiner — Mamadou Diallo

(74) *Attorney, Agent, or Firm* — Murphy, Bilak & Homiller, PLLC

(57) **ABSTRACT**

A semiconductor package includes a mold body having a first main face, a second main face opposite to the first main face and side faces connecting the first and second main faces, a first semiconductor module including a plurality of first semiconductor chips and a first encapsulation layer disposed above the first semiconductor chips, and a second semiconductor module disposed above the first semiconductor module. The second semiconductor module includes a plurality of second semiconductor channels and a second encapsulation layer disposed above the second semiconductor channels. The semiconductor package further includes a plurality of external connectors extending through one or more of the side faces of the mold body.

17 Claims, 3 Drawing Sheets



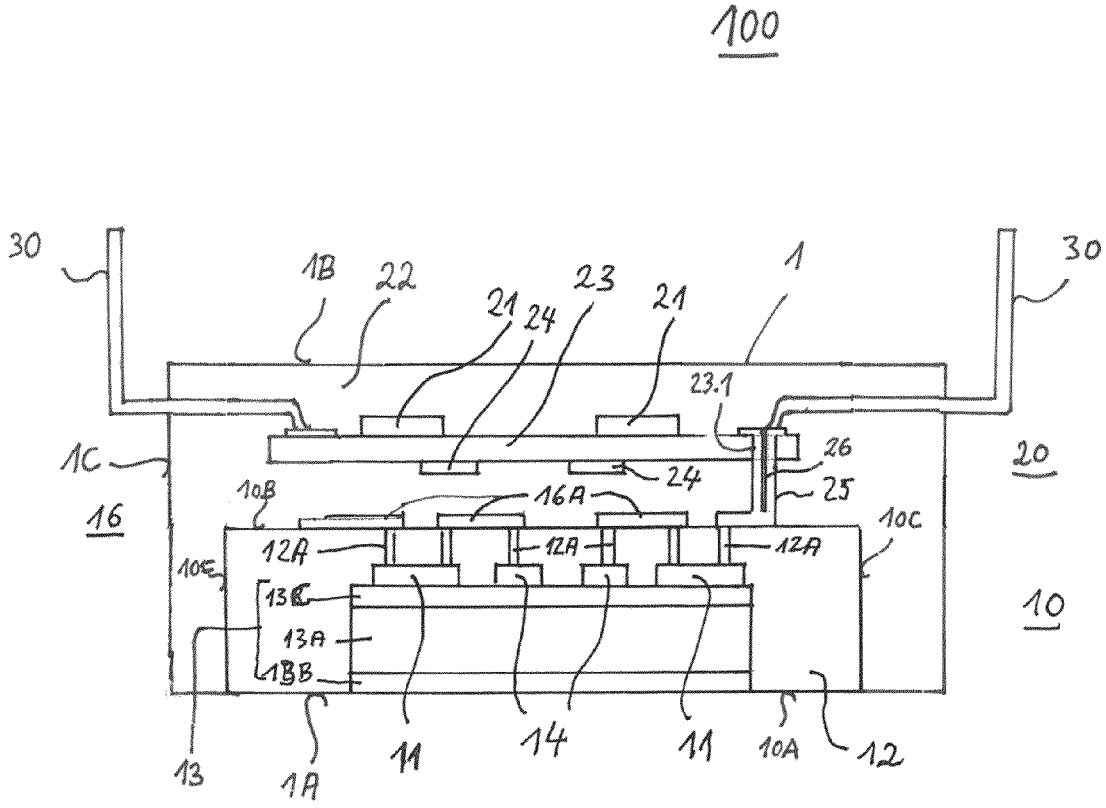

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Fig. 1

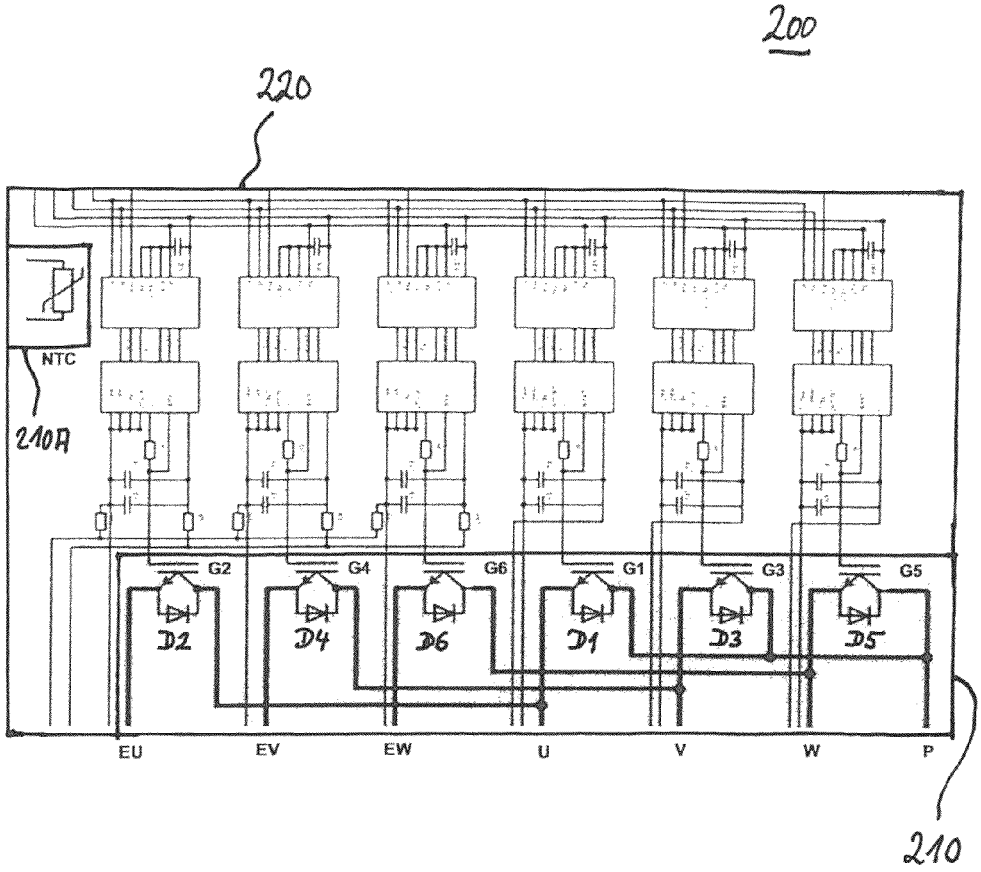
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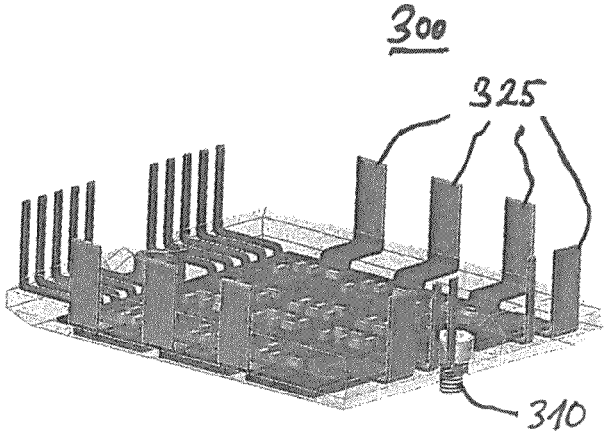
Fig. 2



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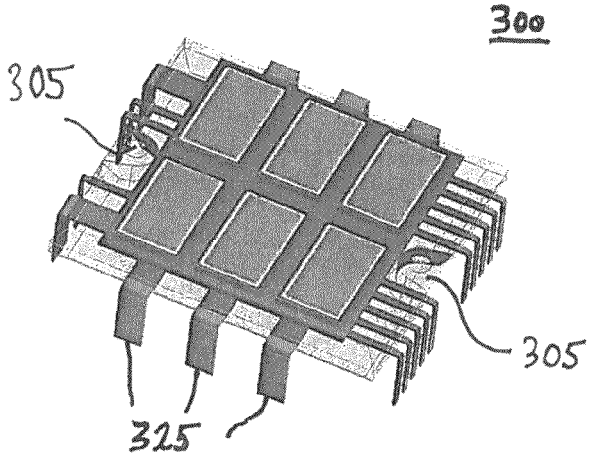

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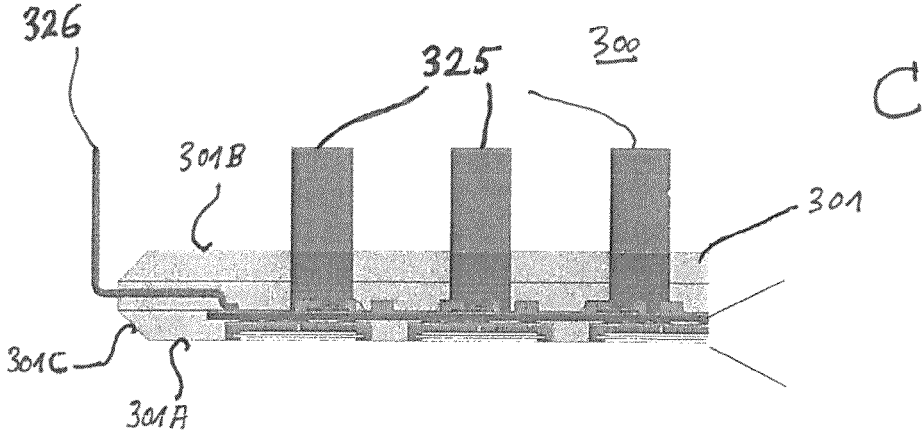

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Fig. 3

SEMICONDUCTOR PACKAGE COMPRISING TWO SEMICONDUCTOR MODULES AND LATERALLY EXTENDING CONNECTORS

TECHNICAL FIELD

Examples described herein generally relate to semiconductor packages and, more particularly, to semiconductor packages such as those comprising a semiconductor transistor module and a semiconductor driver module, and to a method for fabricating a semiconductor package.

BACKGROUND

In many electronic systems it is necessary to employ converters like DC/DC converters, AC/DC converters, DC/AC converters, or frequency converters in order to generate the currents, voltages and/or frequencies to be used by an electronic circuit, like, for example, a motor driving circuit. The converter circuits as mentioned before typically comprise one or more half-bridge circuits, each provided by two semiconductor power switches, such as e.g. power MOSFET devices, and further components such as diodes connected in parallel to the transistor devices, and passive components such as an inductance and a capacitance. The switching of the power MOSFET devices can be controlled by one or more semiconductor driver chips. The assembly of the converter circuit and the assembly of semiconductor driver chips and also the individual components incorporated in these assemblies can in principle be provided as individual components which are mounted on a printed circuit board (PCB). There is, however, a general tendency to save space on the PCB and therefore to provide integrated semiconductor devices having short interconnections between the individual components to reduce switching losses and parasitic inductances.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of examples and are incorporated in and constitute a part of this specification. The drawings illustrate examples and together with the description serve to explain principles of examples. Other examples and many of the intended advantages of examples will be readily appreciated as they become better understood by reference to the following detailed description. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

FIG. **1** shows a schematic cross-sectional side view representation of a semiconductor package according to an example.

FIG. **2** shows a schematic circuit representation of a semiconductor converter circuit and a semiconductor driver circuit connected to the semiconductor converter circuit.

FIGS. **3**A, B and C show a perspective representation (FIG. **3**A), another perspective representation (FIG. **3**B), and a cross-sectional side view representation (FIG. **3**C) of a semiconductor package according to an example.

DETAILED DESCRIPTION

The aspects and examples are now described with reference to the drawings, wherein like reference numerals are generally utilized to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of one or more aspects of the examples. It may

be evident, however, to one skilled in the art that one or more aspects of the examples may be practiced with a lesser degree of the specific details. In other instances, known structures and elements are shown in schematic form in order to facilitate describing one or more aspects of the examples. It is to be understood that other examples may be utilized and structural or logical changes may be made without departing from the scope of the present invention. It should be noted further that the drawings are not to scale or not necessarily to scale.

In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific aspects in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," etc., may be used with reference to the orientation of the figures being described. Since components of described devices may be positioned in a number of different orientations, the directional terminology may be used for purposes of illustration and is in no way limiting. It is understood that other aspects may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

In addition, while a particular feature or aspect of an example may be disclosed with respect to only one of several implementations, such feature or aspect may be combined with one or more other features or aspects of the other implementations as may be desired and advantageous for any given or particular application. Furthermore, to the extent that the terms "include", "have", "with" or other variants thereof are used in either the detailed description or the claims, such terms are intended to be inclusive in a manner similar to the term "comprise". The terms "coupled" and "connected", along with derivatives may be used. It should be understood that these terms may be used to indicate that two elements co-operate or interact with each other regardless whether they are in direct physical or electrical contact, or they are not in direct contact with each other. Also, the term "exemplary" is merely meant as an example, rather than the best or optimal. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

The examples of a semiconductor package and a method for fabricating a semiconductor package may use various types of transistor devices. The examples may use transistor devices embodied in semiconductor dies or semiconductor chips wherein the semiconductor dies or semiconductor chips may be provided in a form of a block of semiconducting material as fabricated from a semiconductor wafer and diced out from the semiconductor wafer, or in another form in which further process steps have been carried out like, for example, applying an encapsulation layer to the semiconductor die or semiconductor chip. The examples may also use horizontal or vertical transistor devices wherein those structures may be provided in a form in which all contact elements of the transistor device are provided on one of the main faces of the semiconductor die (horizontal transistor structures) or in a form in which at least one electrical contact element is arranged on a first main face of the semiconductor die and at least one other electrical contact element is arranged on a second main face opposite to the main face of the semiconductor die (vertical transistor structures) like, for example, MOS transistor structures or IGBT (Insulated Gate Bipolar Transistor) structures. Insofar as the transistor chips are configured as power transistor chips, the examples of a semicon-

ductor package disclosed further below can be classified as intelligent power modules (IPM).

In any case the semiconductor dies or semiconductor chips may comprise contact elements or contact pads on one or more of their outer surfaces wherein the contact elements serve for electrically contacting the semiconductor dies. The contact elements may have any desired form or shape. They can, for example, have the form of lands, i.e. flat contact layers on an outer surface of the semiconductor die. The contact elements or contact pads may be made from any electrically conducting material, e.g. from a metal as aluminum, gold, or copper, for example, or a metal alloy, or an electrically conducting organic material, or an electrically conducting semiconductor material. The contact elements may also be formed as layer stacks of one or more of the above-mentioned materials.

The examples of a semiconductor package may comprise an encapsulant or encapsulating material having the semiconductor transistor chips and the at least one semiconductor driver chip embedded therein. The encapsulating material can be any electrically insulating material like, for example, any kind of molding material, any kind of resin material, or any kind of epoxy material. The encapsulating material can also be a polymer material, a polyimide material, a thermoplast material, a silicone material, a ceramic material, and a glass material. The encapsulating material may also comprise any of the above-mentioned materials and further include filler materials embedded therein like, for example, thermally conductive increments. These filler increments can be made of AlO or Al_2O_3, AlN, BN, or SiN, for example. Furthermore the filler increments may have the shape of fibers and can be made of carbon fibers or nanotubes, for example. The examples of a semiconductor package may also comprise two different encapsulating materials, one of which having the semiconductor transistor chips embedded therein and the other one of which having the at least one semiconductor driver chip embedded therein.

FIG. **1** shows a cross-sectional side view representation of a semiconductor package according to an example. The semiconductor package **100** comprises a mold body **1** comprising a first main face **1**A, a second main face **1**B opposite to the first main face **1**A, and side faces **1**C connecting the first and second main faces **1**A and **1**B. The semiconductor package **100** further comprises a first semiconductor module **10** and a second semiconductor module **20** disposed above the first semiconductor module **10**. The first semiconductor module **10** may comprise a first (lower) main face **10**A, a second (upper) main face **10**B opposite to the first main face **10**A, and side faces **10**C connecting the first and second main faces **10**A and **10**B. In case of a rectangular or cuboid shape of the first semiconductor module **10**, the first semiconductor module **10** comprises four side faces **10**C. As mentioned before, the second semiconductor module **20** is disposed above the first semiconductor module. As shown in FIG. **1**, "above" can have a meaning that the second encapsulation layer **22** of the second semiconductor module **20** covers the first encapsulation layer **12** on its second main face **10**B and on its side faces **10**C, in particular is directly attached to the second main face **10**B and the side faces **10**C, and the lower surface of the second encapsulation layer **22** is flush with the first main face **10**A of the first semiconductor module **10**. "Above" can also have a different meaning, namely that the second encapsulation layer **22** of the second semiconductor module **20** only covers the second main face **10**B but not the side faces **10**C of the first semiconductor module **10**.

The first semiconductor module **10** comprises a plurality of first semiconductor chips **11** and a first encapsulation layer **12** disposed above the first semiconductor chips **11**. The second semiconductor module **20** may comprise a plurality of second semiconductor chips **21** and a second encapsulation layer **22** disposed above the second semiconductor chips **21**. The second semiconductor chips **21** may be electrically connected to the first semiconductor chips **11**. The first semiconductor chips **11** may be comprised of semiconductor transistor chips **11** and the second semiconductor chips **21** may be comprised of semiconductor driver chips **21**. The semiconductor driver chips **21** may be electrically connected to control electrodes, i.e. gate electrodes, of the semiconductor transistor chips **11** and the semiconductor driver chips **21** may be configured to drive the semiconductor transistor chips **11**.

It should be mentioned further that instead of the plurality of separate semiconductor driver chips **21** as depicted in FIG. **1**, also one single semiconductor driver chip can be provided, wherein the single semiconductor driver chip comprises a plurality of semiconductor driver channels integrated on the single semiconductor driver chip. Hence for the purpose of this application the terms "semiconductor driver channels **21**" and "semiconductor driver chips **21**" are meant to be interchangeable in the above sense.

The semiconductor package **100** further comprises a plurality of external connectors **30** extending through the side faces **1**C of the mold body **1**. In FIG. **1** the external connectors **30** are shown to pass through the side faces **1**C in an upper portion of the side faces **1**C, respectively. However, an example of a semiconductor package described further below shows that the external connectors may also pass through the side faces at or around a center or center portion of the side faces **1**C.

According to an example of the semiconductor package **100**, the external connectors **30** may be divided in two groups. A first group of the external connectors **30** may be electrically connected to the first semiconductor module **10**, and a second group of the external connectors **30** may be electrically connected to the second semiconductor module **20**. FIG. **1** shows two external connectors **30**. The external connector **30** shown on the left-hand side of FIG. **1** is electrically connected to the second semiconductor module **20**, and the external connector **30** shown on the right-hand side of FIG. **1** is electrically connected to the first semiconductor module **10**. To this end, all external connectors **30** may be mechanically connected to the second semiconductor module **20**, wherein the second semiconductor module **20** may comprise a printed circuit board **23** and the external connectors **30** may be mechanically connected to the printed circuit board **23**. The printed circuit board **23** may comprise through-connections **23.1** and the first group of the external connectors **30** may be connected to the through-connections **23.1** in order to be able to be connected with the first semiconductor module **10**.

According to an example of the semiconductor package **100** of FIG. **1**, each one of the external connectors **30** comprises a first horizontal portion being disposed mainly within the mold body **1** and a second vertical portion being disposed outside of the mold body **1**, wherein the second portion is bent in a right angle with respect to the first portion. According to an example, the first portions of all of the external connectors **30** lie in one and the same plane. According to an example, the second portions of the external connectors **30** comprise one or more of equal direction and equal length. The latter means that outer end portions of the external connectors lie in one and the same plane. According to the representation in FIG. **1** the second portion of the external connectors **30** is bent in a right angle. It should be added, however, that the second portion can also be bent in another angle and some or all of the

external connectors **30** need to be bent at all and the second portions of the external connectors **30** can be bent in a different and with different angles.

According to an example of the semiconductor package, the mold body **1** comprises two vertical through-holes (not shown in FIG. **1**) formed in two opposing side edges of the mold body **1**, each one of the two through-holes extending from the first main face of the mold body to the second main face of the mold body. The purpose of these two through-holes is to fix the semiconductor package to a substrate like, for example, a heat spreader by means of screws inserted in the through-holes.

According to an example of the semiconductor package **100** of FIG. **1**, the first semiconductor module **10** comprises a carrier **13**. According to an example the carrier **13** comprises a substrate **13**A comprising an insulating, dielectric or ceramic layer or tile, and a first metallic layer **13**B on a lower surface of the substrate **13**A and a second metallic layer **13**C on an upper surface of the substrate **13**A. According to an example the carrier **13** may comprise one or more of a direct copper bonded (DCB) substrate, a direct aluminum bonded (DAB) substrate, and an active metal brazing substrate, wherein the substrate may comprise a ceramic layer, in particular one or more of AlO, AlN, Al_2O_3, or a dielectric layer, in particular Si_3N_4. According to an example, the carrier **13** may comprise a first upper surface, a second lower surface opposite to the first upper surface, and side faces connecting the first and second surfaces, wherein the first encapsulation layer **12** may cover the first upper surface and the side faces of the carrier **13**. According to an example, the carrier **13** may comprise a substrate **13**A which may be an inorganic or an organic substrate. The core of the substrate **13**A, in particular of the organic substrate, may comprise a thermal conductivity better than 1 W/mK. According to an example, the carrier **13** may comprise a thickness in a range from 0.1 mm to 0.3 mm, in particular in a range from 0.15 mm to 0.25 mm.

According to an example of the semiconductor package **100** of FIG. **1**, the first semiconductor module **10** further comprises a plurality of semiconductor diode chips **14**, which can be configured as flyback diodes. According to an example, each one of the semiconductor transistor chips **11** is connected with one of the semiconductor diode chips **14** in parallel. According to an example, the first semiconductor module **10** further comprises a metallization layer **16** comprising a plurality of metallic areas **16**A forming electrical connections between selected ones of the semiconductor transistor chips **11** and the semiconductor diode chips **14**. In addition the first encapsulation layer **12** may comprise via connections **12**A connecting the metallic areas **16**A with selected ones of the semiconductor transistor chips **11** and the semiconductor diode chips **14**. The via connections **12**A will be described in more detail below, in particular they may comprise lateral diameters greater than 50 μm.

According to an example of the semiconductor package **100** of FIG. **1**, the first semiconductor chips **11** are comprised of semiconductor transistor chips, in particular semiconductor power transistor chips, and the second semiconductor chips **21** are comprised of semiconductor driver chips **21**. According to an example, the semiconductor transistor chips **11** are interconnected to form an AC/AC converter circuit, an AC/DC converter circuit, a DC/AC converter circuit, a frequency converter, or a DC/DC converter circuit.

According to an example of the semiconductor package **100** of FIG. **1**, the first semiconductor module **10** further comprises semiconductor diode chips **14**, wherein each one of the semiconductor diode chips **14** may be connected in parallel to one of the semiconductor transistor chips **11**.

According to an example of the semiconductor package **100** of FIG. **1**, one or more of the semiconductor transistor chips **11** and the semiconductor diode chips **14** comprise a thickness in a range from 5 μm to 700 μm, in particular from 30 μm to 100 μm, in particular from 50 μm to 80 μm.

According to an example of the semiconductor package **100** of FIG. **1**, the semiconductor transistor chips **11** each comprise one or more of a power transistor, a vertical transistor, an MOS transistor, and an insulated gate bipolar transistor (IGBT). According to an example, the semiconductor material of one or more of the semiconductor transistor chips **11** and the semiconductor diode chips **14** may be based on Si, GaN, SiC or any other semiconductor material.

According to an example of the semiconductor package **100** of FIG. **1**, the encapsulation layer **12** comprises a thickness in a range from 0.05 mm to 1.5 mm above the upper surface of the carrier **13**. According to an example, the first encapsulation layer **12** may comprise a thickness in a range from 200 μm to 300 μm above the first, upper main face of the semiconductor transistor chips **11**.

The semiconductor package **100** may be configured in two different variants with respect to the first semiconductor module **10**. Reference is made in this respect to U.S. patent application Ser. No. 13/974,583 (the "prior patent application") of one and the same Assignee as the present application, wherein the disclosure of the prior patent application is incorporated in its entirety into the present application. A first variant maybe entitled "common DCB approach" and is represented by FIG. **1** of the present application wherein the first semiconductor module **10** comprises one contiguous carrier **13** enclosed at five sides (four side faces and the top main face) by the first encapsulation layer **12**. In particular such a first semiconductor module **10** may comprise six semiconductor power transistors, in particular six IGBT transistors, and six semiconductor diodes. A second variant maybe entitled "segmented DCB approach" wherein the first semiconductor module comprises a number of separate modules such as those shown in FIG. **5** of the prior patent application. These separate modules may each be constructed in the same way as the first semiconductor module **10** shown in FIG. **1**, namely a carrier **13** embedded in a first encapsulation layer **12**, wherein the number of separate modules are separated from each other by the second encapsulation layer **22** so that as a result each one of the separate modules is covered on all five sides (four side faces and one top face) by the second encapsulation layer **22**.

According to an example of the semiconductor package **100** of FIG. **1**, one or more of the first encapsulation layer **12** and the second encapsulation layer **22** comprises one or more of a polymer material, a mold compound material, a resin material, an epoxy-resin material, an acrylate material, a polyimide material, and a silicone-based material. According to an example, the first and second encapsulation layers **12** and **22** comprise different materials.

According to an example of the semiconductor package **100** of FIG. **1**, the first encapsulation layer **12** comprises via connections **12**A connecting the metallic areas **16**A of the metallization layer **16** with selected ones of the semiconductor transistor chips **11** and the semiconductor diode chips **14**. The via connections **12**A may comprise lateral diameters in a range from 0.05 mm to 1 mm, in particular from 0.3 mm to 0.7 mm. According to an example, the via connections **12**A comprise a ratio of height to width in a range from 0 to 3, preferably in a range from 0.3 to 3.

According to an example of the semiconductor package **100** of FIG. **1**, the via connections **12**A comprise via holes through the encapsulation layer **12**, the via holes being filled

completely or in part with an electrically conducting material like, for example, a metal as, for example, copper. The electrically conducting material can be filled into the via holes in such a way that the via holes are not completely filled by the material but instead the material only covers the walls of the via holes with a thickness less than half the diameter of the via holes.

According to an example of the semiconductor package **100** of FIG. **1**, the first semiconductor module **10** comprises one or more half-bridge circuits wherein in each half-bridge circuit two semiconductor transistor chips **11** are connected in series. In particular, the first semiconductor module **10** may comprise six semiconductor transistor chips **11** wherein two respective semiconductor transistor chips **11** are connected in series to form three half-bridge circuits.

According to an example of the semiconductor package **100** of FIG. **1**, each one of the semiconductor transistor chips **11** is connected with one of the semiconductor diode chips **14** in parallel. In particular, the first semiconductor module **10** may comprise six semiconductor transistor chips **11** and six semiconductor diode chips **14** each of them connected in parallel to one of the semiconductor transistor chips **11**.

According to an example of the semiconductor package **100** of FIG. **1**, the second semiconductor module **20** comprises a printed circuit board **23** and the semiconductor driver chips **21** are connected to the printed circuit board **23**. According to an example, the printed circuit board **23** is disposed in a distance from the first semiconductor module **10**, and the second encapsulation layer **22** is disposed in an intermediate space between the printed circuit board **23** and the first semiconductor module **10**. According to an example, the printed circuit board **23** is completely embedded within the second encapsulation layer **22**.

According to an example of the semiconductor package **100** of FIG. **1**, the semiconductor driver chips **21** can be connected only on an upper surface of the printed circuit board **23**. It is also possible that the semiconductor driver chips **21** are only connected to the lower surface of the printed circuit board **23**. It is also possible that the semiconductor driver chips **21** are connected on both the upper and the lower surfaces of the printed circuit board **23**.

According to an example of the semiconductor package **100** of FIG. **1**, the second semiconductor module **20** comprises a plurality of passive devices **24** like, for example, resistors, capacitors, inductors and the like. According to an example, the passive devices **24** can be connected only to a lower surface of the printed circuit board **23**. They also can be connected only to an upper surface of the printed circuit board **23**. A further possibility is that the passive devices **24** can be connected to the lower surface as well as to the upper surface of the printed circuit board **23**.

According to an example of the semiconductor package **100** of FIG. **1**, electrical connections between the first semiconductor module **10** and the second semiconductor module **20** are provided by sleeves **25** and metallic pins **26** inserted into the sleeves **25**. The sleeves **25** can be embedded within the second encapsulation layer **22** so that they are surrounded laterally on all sides by the second encapsulation layer **22**. The sleeves **25** can have circular cross-section, for example. The printed circuit board **23** may comprise through-connectors **23.1** at predetermined locations thereof so that, wherever necessary, an electrical through-connection can be formed by connecting a sleeve **26** with the inserted pin **25** with a through-connector **23.1**, e.g. for providing an electrical connection between a semiconductor driver chip **21** connected to an upper surface of the printed circuit board **23** with a semiconductor transistor chip **11** or for connecting a semiconductor transistor chip **11** to an external connector **30**. By such an electrical connection an electrical output current out of one of the half-bridge circuits may be provided, for example, or an input voltage may be supplied to one of the half-bridge circuits.

FIG. **2** shows an example of a circuitry which can be realized by a semiconductor package as described above. The circuit design shown in FIG. **2** represents a three-phase inverter circuit **200** for generating three-phase alternating currents which can be used, for example, for driving an electric motor. The circuit **200** comprises a transistor circuit **210** comprising six transistors G**1**-G**6** each one of which may be connected in parallel to one of six diodes D**1**-D**6**. The transistor circuit **210** may be further divided in three half-bridge circuits, each one of the half-bridge circuits providing one phase of the three-phase currents. In particular, a first half-bridge circuit is formed by a series connection of the transistors G**1** and G**2** providing a first current U at a node between the transistors G**1** and G**2**, a second half-bridge circuit is formed by a series connection of the transistors G**3** and G**4** providing a second current V at a node between the transistors G**3** and G**4**, and a third half-bridge circuit is formed by a series connection of the transistors G**5** and G**6** providing a third current W at a node between the transistors G**5** and G**6**. Each one of the three half-bridge circuits is provided with one of three voltages EU, EV and EW and each one of these voltages is input at a source terminal of one of the transistors of the respective half-bridge circuit. The drain contact of the respective other transistors of the half-bridge circuits are connected to one common potential P. The circuit **200** further comprises a driver circuit **220** comprising driver circuit chips. Each one of the transistors G**1**-G**6** is driven by two driver circuit chips which are depicted vertically above the transistors G**1**-G**6**, respectively. The transistor circuit **210** may be incorporated within the first semiconductor module **10** shown in FIG. **1** and the driver circuit **220** may be incorporated within the second semiconductor module **20** shown in FIG. **1**. In addition an NTC (negative temperature coefficient) temperature sensor (**210**A, NTC) may be provided which is shown on the left side on top of the circuit representation but in fact may be part of the first semiconductor module comprising the transistor circuit **210** as it may be important to monitor the temperature of the first semiconductor module in operation of the device.

FIGS. **3**A,B and C show an example of a semiconductor package **300** in a first perspective view (FIG. **3**A), a second perspective view (FIG. **3**B), and a cross-sectional side view (FIG. **3**C). The semiconductor package **300** comprises a mold body **301** comprising a first main face **301**A, a second main face **301**B, and side faces **301**C connecting the first and second main faces **301**A and **301**B. The side faces **301**C may be comprised of two inclined faces each one of which being connected with one of the first and second main faces **301**A and **301**B, and a vertical face connecting the two inclined faces. The semiconductor package **300** further comprises a plurality of first external connectors **325** and second external connectors **326**, all of them extending through one of the four side faces **301**C of the mold body **301** and after being bent in a right angle extending in one and the same direction. As already explained in connection with FIG. **1**, there are two types of external connectors, namely first external connectors **325** which are electrically connected to the first semiconductor module and which are connected each one with one of the terminals U, V, W, EU, EV, EW or P as shown in the circuit diagram of FIG. **2**. The second external connectors **326** are electrically connected with the second semiconductor module to provide power supply and control signals to the semiconductor driver chips of the second semiconductor module.

The first and second external connectors **325** and **326** may be formed as strip-like connectors of any kind of metallic material like, for example, copper or a copper alloy. The first external connectors **325** may have a greater strip width in order to enhance their ampacity. The mold body **301** may further comprise vertical through-holes **305** formed in opposing side edges for the purpose of mounting the semiconductor package **300** by screws **310** to a substrate like, for example, a heat spreader.

While the invention has been illustrated and described with respect to one or more implementations, alterations and/or modifications may be made to the illustrated examples without departing from the spirit and scope of the appended claims. In particular regard to the various functions performed by the above described components or structures (assemblies, devices, circuits, systems, etc.), the terms (including a reference to a "means") used to describe such components are intended to correspond, unless otherwise indicated, to any component or structure which performs the specified function of the described component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure which performs the function in the herein illustrated exemplary implementations of the invention.

What is claimed is:

1. A semiconductor package, comprising:
- a mold body comprising a first main face, a second main face opposite to the first main face and side faces connecting the first and second main faces;
- a first semiconductor module comprising a plurality of first semiconductor chips and a first encapsulation layer disposed above the first semiconductor chips;
- a second semiconductor module disposed above the first semiconductor module, the second semiconductor module comprising at least one second semiconductor chip and a second encapsulation layer disposed above the at least one second semiconductor chip; and
- a plurality of external connectors extending through one or more of the side faces of the mold body,
- wherein the external connectors are mechanically connected to the second semiconductor module.

2. The semiconductor package according to claim **1**, wherein a first group of the external connectors is electrically connected to the first semiconductor module, and a second group of the external connectors is electrically connected to the second semiconductor module.

3. The semiconductor package according to claim **1**, wherein the second semiconductor module comprises a printed circuit board and the at least one second semiconductor chip is connected to the printed circuit board.

4. The semiconductor package according to claim **3**, wherein the external connectors are mechanically connected to the printed circuit board.

5. The semiconductor package according to claim **3**, wherein the printed circuit board comprises through-connections and a group of the external connectors is connected to the through-connections.

6. The semiconductor package according to claim **1**, wherein each one of the external connectors comprises a first portion disposed mainly within the mold body, and a second portion disposed outside of the mold body, and wherein the second portion is bent at a right angle with respect to the first portions.

7. The semiconductor package according to claim **6**, wherein the first portions of the external connectors lie in one and the same plane.

8. The semiconductor package according to claim **6**, wherein the second portions of the external connectors comprise one or more of equal direction and equal length.

9. The semiconductor package according to claim **1**, wherein the mold body comprises two vertical through-holes formed in two opposing side edges of the mold body, each one of the through-holes extending from the first main face of the mold body to the second main face of the mold body.

10. The semiconductor package according to claim **1**, wherein the first semiconductor chips comprise semiconductor transistor chips and the at least one second semiconductor chip comprises a plurality of semiconductor driver channels.

11. The semiconductor package according to claim **10**, wherein the semiconductor transistor chips are connected to form an AC/AC converter circuit, an AC/DC converter circuit, a DC/AC converter circuit, a frequency converter, or a DC/DC converter circuit.

12. A semiconductor package, comprising:
- a mold body comprising a first main face, a second main face opposite to the first main face and side faces connecting the first and second main faces;
- a semiconductor power module comprising a plurality of semiconductor power transistor chips;
- a semiconductor driver module comprising a plurality of semiconductor driver channels, the semiconductor driver module being disposed above and attached to the semiconductor power module; and
- a plurality of external connectors extending through one or more side faces of the mold body,
- wherein the semiconductor power module further comprises a first encapsulation layer disposed above the semiconductor power transistor chips and a plurality of sub-modules separated from each other by the first encapsulation layer,
- the semiconductor package further comprising:
  - a redistribution layer disposed above the first encapsulation layer, the redistribution layer comprising metallic layers connecting selected ones of the semiconductor power transistor chips.

13. The semiconductor package according to claim **12**, wherein
- the mold body comprises four side faces and the external connectors extend through all four side faces of the mold body.

14. The semiconductor package according to claim **12**, wherein
- each one of the semiconductor power transistor chips is connected to one or two semiconductor driver chips.

15. A semiconductor package, comprising:
- a mold body comprising a first main face, a second main face opposite to the first main face and side faces connecting the first and second main faces;
- a first semiconductor module comprising a plurality of first semiconductor chips and a first encapsulation layer disposed above the first semiconductor chips;
- a second semiconductor module disposed above the first semiconductor module, the second semiconductor module comprising at least one second semiconductor chip and a second encapsulation layer disposed above the at least one second semiconductor chip; and
- a plurality of external connectors extending through one or more of the side faces of the mold body,
- wherein the second semiconductor module comprises a printed circuit board and the at least one second semiconductor chip is connected to the printed circuit board,

wherein the printed circuit board comprises through-connections and a group of the external connectors is connected to the through-connections.

16. A semiconductor package, comprising:

a mold body comprising a first main face, a second main face opposite to the first main face and side faces connecting the first and second main faces;

a first semiconductor module comprising a plurality of first semiconductor chips and a first encapsulation layer disposed above the first semiconductor chips;

a second semiconductor module disposed above the first semiconductor module, the second semiconductor module comprising at least one second semiconductor chip and a second encapsulation layer disposed above the at least one second semiconductor chip; and

a plurality of external connectors extending through one or more of the side faces of the mold body,

wherein each one of the external connectors comprises a first portion disposed mainly within the mold body, and a second portion disposed outside of the mold body,

wherein the second portion is bent at a right angle with respect to the first portions.

17. A semiconductor package, comprising:

a mold body comprising a first main face, a second main face opposite to the first main face and side faces connecting the first and second main faces;

a first semiconductor module comprising a plurality of first semiconductor chips and a first encapsulation layer disposed above the first semiconductor chips;

a second semiconductor module disposed above the first semiconductor module, the second semiconductor module comprising at least one second semiconductor chip and a second encapsulation layer disposed above the at least one second semiconductor chip; and

a plurality of external connectors extending through one or more of the side faces of the mold body,

wherein the mold body comprises two vertical through-holes formed in two opposing side edges of the mold body, each one of the through-holes extending from the first main face of the mold body to the second main face of the mold body.

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